INDUSTRY STANDARD PANELS
13.3", 14.1" and 15.0"
Mounting & Top Level Interface Requirements

Version 2
September, 2001

Purpose

To establish a set of displays with standard dimensions and interface characteristics so that both the notebook and panel supplier industries will be able to manage the volatile LCD supply and demand in an easier fashion. This effort will enable panels from various LCD suppliers to be used in most notebooks *(or other products utilizing these standard panels)* that are designed around these Standard Panels without having to change either the notebook/product tooling or the LCD module tooling.

Summary

To date, the notebook and panel industry has been plagued by an overabundance of unique/custom designs from the many LCD suppliers in the industry. This has in turn, forced the notebook OEMs and other end-product users to change packaging, interface design, and tooling literally every time a new panel supplier or module has been used. This leads to schedule slippages, missed market opportunities, and logistics and product obsolescence problems. Similarly, many times this problem has blocked some LCD manufacturers from being considered as a potential supplier due to the magnitude of changes their design would force on the notebook end product. As more panel suppliers come on line in the near future, this style of independent designs would only increase this problem for both the notebook OEMs as well as the LCD suppliers. In an attempt to lessen this problem, these requirements are being established with the aid of both notebook OEMs and LCD panel suppliers.

Version 2 incorporates form-factor changes that will enable the development of thinner panels aimed at the ultra-portable products, while it maintains mounting compatibility with initial standard thickness designs targeted at performance products.

No Warranty The following specification has NOT BEEN DEVELOPED BY VESA, NOR DOES VESA ASSERT OWNERSHIP RIGHTS IN THIS SPECIFICATION. It is being made available at the VESA site because it has (i) been developed by third parties operating in an informal collaborative process, which is no longer operative, and (ii) has become a widely implemented "de facto" standard.

This specification is being published at the VESA site AS IS, WITH NO WARRANTY, EXPRESS OR IMPLIED, OF ANY KIND WHATSOEVER, INCLUDING WITH RESPECT TO THE OWNERSHIP OR NON-INFRINGEMENT OF THE SPECIFICATION, OR AS TO ITS ACCURACY, COMPLETENESS, SUITABILITY OR USEFULNESS. Any copying or implementation of this specification shall be solely at the risk of the party taking such action, and VESA shall have no liability whatsoever with respect to the consequences of such conduct, including with respect to any intellectual property owner alleging infringement of its copyright(s), patent(s) or other rights. VESA assumes no obligation to notify any implementer of any subsequent allegations of infringement or other violations.

Reservation of Intellectual Property rights The contributors to this document acknowledge that each contributor may have patent rights. Except for the rights expressly provided by this Agreement, no Promoter grants or receives, by implication, estoppels or otherwise, any rights under any patents or other intellectual property.

Trademarks

All trademarks used within this document are the property of their respective owners. VESA, DDC/CI, E-EDID are trademarks of Video Electronics Standard Association. LVDS is a trademark of National Semiconductor. JAE is a trademark of Japan Aviation Electronics Industry, Ltd. I^2C is a trademark of Philips. PC99 is a trademark of Microsoft Corporation.

Support for this Standard

The Standard Panel Working Group, which consists of many of the major notebook suppliers, in conjunction with many of the leading LCD suppliers, has established these mechanical and electrical requirements defined herein. These requirements have been refined through a number of proposal/feedback review cycles with these suppliers.

This document is intended as a reference document only for both notebook OEMs and panel suppliers. Users of this document should not base final end-product designs (notebook or other) on this document, but instead should utilize the display supplier's detailed drawings and specifications for full documentation.

1. OVERVIEW

1.1 Summary

This document defines selected electrical interface requirements and mechanical dimensions for a series of industry compatible panels for XGA *(1024x768),* SXGA+ *(1400x1050),* UXGA *(1600x1200)* and QXGA *(2048x1536)* resolution LCD panels. This document supports the development of thinner panels targeted at the ultra-mobile products (Style B), as well as maintaining compatibility with the standard thickness models (Style A) targeted for performance products. Through the DDC/EEDID interface, it also provides graphics controller BIOS and driver support, and provides support for Microsoft PC99 and future PCxxxx requirements.

1.2 Background

With most panels used in portable computer designs today, the notebook OEM has to have different interface cables, plastic or magnesium enclosures, bezels, bracket assemblies, and EMI shields for every panel used. For each of these parts, there are associated tooling changes required and schedule impacts relative to these tooling changes, to support the use of the different panels. Additionally, the associated documentation and logistics impacts for these different configurations are staggering. Many times these changes, and schedule impacts that would be caused by these changes, eliminate many panel suppliers from being considered as potential second sources.

1.3 Standard Objectives

This document establishes common panels for the three display sizes, and two form-factor styles for each size that enables a Standard Panel to be mounted in any system that has been designed to accept the maximum size Standard Panel of either of the two styles defined. The Standard Panel method of dimensioning has been developed to allow panel suppliers a method of providing product differentiation and still meet the intent of transparent usage across different platforms.

Additionally, with the various requirements of PC99 and future PCxxxx versions, the incorporation of E-EDID will allow transparent usage with minimum changes to system BIOS or drivers. The end objective is to specify panel-timing requirement so that no BIOS or driver changes are required with the use of a new panel.

2. REFERENCE DOCUMENTS

The following documents form a part of this specification to the extent specified herein. The user of this document is advised to ensure they have the latest versions of these reference standards and documents.

- VESA Display Data Channel Standard, DDC2B
- VESA Enhanced Extended Display Identification Data
- Philips I^2C Bus Specification - Data Handbook I^2C Peripherals for Microcontrollers 1/92
- TIA/EIA-644 ELECTRICAL CHARACTERISTICS OF LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INTERFACE CIRCUITS

3. SYSTEM ELECTRICAL INTERFACE REQUIREMENTS

The panel's electrical interface to the system consists of two physical electrical interfaces comprising the Display Data Channel interface, and the system power and LVDS interface which encodes the RGB data and timing/control signals.

3.1 Display Data Channel Requirements

To support notebook-level transparent second source capability and provide support of Microsoft's PCxxxx requirements, the panels shall support I^2C-based Display Data Channel communications. The only level of support required is DDC2B, compatibility with earlier DDC versions is not supported. The Display Data Channel serial interface shall transmit the Enhanced Extended Display Identification Data (E-EDID) containing panel specific data.

3.1.1 DDC2B Physical Layer Electrical Requirements

The DDC interface shall support the full I^2C interface of DDC2B requirements for signals and timing with the exception that the +5VDC monitor interface supply voltage shall be replaced with +3.3VDC.

3.1.2 EDID Logical Layer Requirements

This standard supports VESA Enhanced EDID Structure 1.2. All data fields of structure 1.2 are required to be supported, with the exception of ID serial number, Week of Manufacture, and Year of Manufacture fields, which are optional. It is anticipated that in the near future, as the panel suppliers develop real-time data gathering capabilities on their factory floor, these three fields will then be implemented as well.

3.2 Logic Power and Data/Control Interface

3.2.1 Interface Connector Requirements

The module interface connector for the different resolutions and form-factor styles shall be as defined in Table 1 below. The connector keep-out area for the module shall be designed to support insertion of either a wire-crimp style connector, or the wider flex-cable style connector. Connector keying relative to pin 1 designation shall be as shown in JAE data sheets.

TABLE 1
MODULE INTERFACE CONNECTOR

Form-factor Style	Resolution	Part Number
Style A	XGA	JAE FI-SEB20P-HFxx or JAE FI-SE20P-HFxx or equivalent
	SXGA+ & above	JAE FI-XB30Sx-HFxx or JAE FI-X30S-HFxx or equivalent
Style B	All Resolutions	JAE FI-XB30Sx-HFxx or JAE FI-X30S-HFxx or equivalent

3.2.2 Interface Signal Definition

The interface connector pin assignments for Style A XGA resolution panels are listed in Table 2. The interface connector pin assignments for all Style A panels of SXGA+ resolution and above, and for all Style B panels are listed in Table 3.

3.2.3 Power Sequencing Requirements

To prevent a latch-up or DC operation of the LCD, the panel shall support the following logic power and data/control signal sequencing of Figure 1.

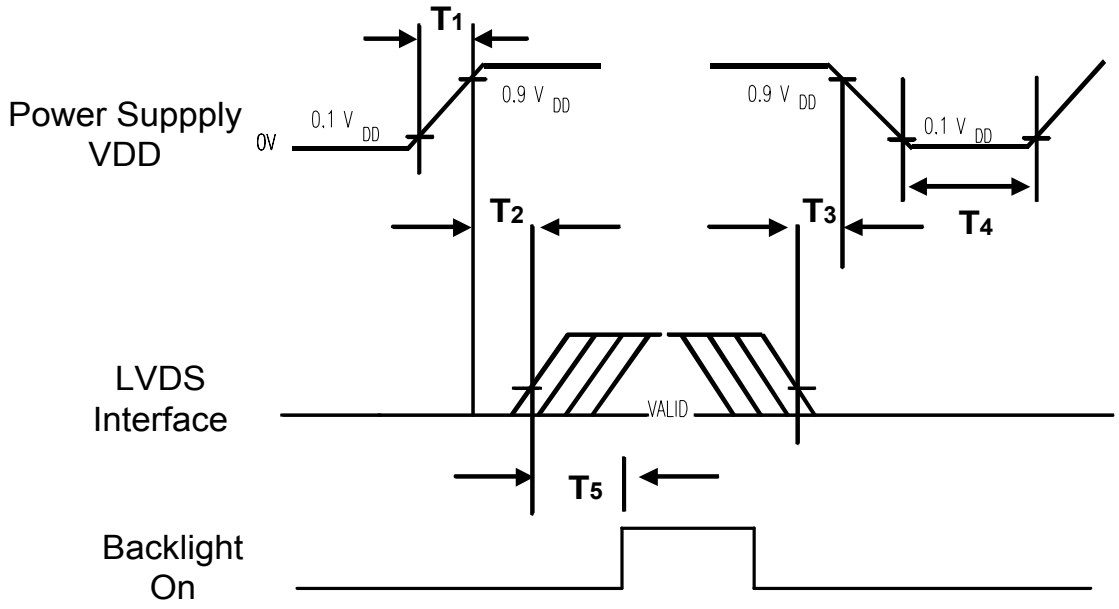
TABLE 2
XGA INTERFACE CABLE PIN ASSIGNMENTS

PIN NO.	SYMBOL	FUNCTION
1	VDD	Power Supply, 3.3 V (typical)
2	VDD	Power Supply, 3.3 V (typical)
3	VSS	Ground
4	VSS	Ground
5	Rin0 -	Negative LVDS differential data input (pixel R0-R5, G0)
6	Rin0 +	Positive LVDS differential data input (pixel R0-R5, G0)
7	VSS	Ground
8	Rin1 -	Negative LVDS differential data input (pixel G1-G5, B0-B1)
9	Rin1 +	Positive LVDS differential data input (pixel G1-G5, B0-B1)
10	VSS	Ground
11	Rin2 -	Negative LVDS differential data input (pixel B2-B5, HS, VS, DE)
12	Rin2 +	Positive LVDS differential data input (pixel B2-B5, HS, VS, DE)
13	VSS	Ground
14	CLK -	Clock Signal (-)
15	CLK +	Clock Signal (+)
16	VSS	Ground
17	V_{EDID}	DDC 3.3V power
18	NC	Reserved for supplier test point
19	Clk_{EDID}	DDC Clock
20	$DATA_{EDID}$	DDC Data

TABLE 3
SXGA+/UXGA/QXGA INTERFACE CABLE PIN ASSIGNMENTS

PIN NO.	SYMBOL	FUNCTION
1	VSS	Ground
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V_{EDID}	DDC 3.3V power
5	*NC*	*Reserved for supplier test point*
6	Clk_{EDID}	DDC Clock
7	$DATA_{EDID}$	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels on SXGA+/UXGA)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels on SXGA+/UXGA)
10	VSS	Ground
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels on SXGA+/UXGA)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels on SXGA+/UXGA)
13	VSS	Ground
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels on SXGA+/UXGA)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels on SXGA+/UXGA)
16	VSS	Ground
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels on SXGA+/UXGA)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels on SXGA+/UXGA)
19	VSS	Ground
20	Even_Rin0-	- LVDS differential data input (even pixels R0-R5, G0) (NC on XGA)
21	Even_Rin0+	+ LVDS differential data input (even pixels R0-R5, G0) (NC on XGA)
22	VSS	Ground
23	Even_Rin1-	- LVDS differential data input (even pixels G1-G5, B0-B1) (NC on XGA)
24	Even_Rin1+	+ LVDS differential data input (even pixels G1-G5, B0-B1) (NC on XGA)
25	VSS	Ground
26	Even_Rin2-	- LVDS differential data input (even pixels B2-B5, HS, VS, DE) (NC on XGA)
27	Even_Rin2+	+ LVDS differential data input (even pixels B2-B5, HS, VS, DE) (NC on XGA)
28	VSS	Ground
29	Even_CLKIN-	- LVDS differential clock input (even pixels) (NC on XGA)
30	Even_CLKIN+	+ LVDS differential clock input (even pixels) (NC on XGA)

FIGURE 1
LOGIC POWER AND LVDS SIGNALS SEQUENCING DIAGRAM



$t_1 \leq 10$ ms $0 \leq t2 \leq 50$ ms $0 \leq t3 \leq 50$ ms 400 ms $\leq t4$ 200 ms $\leq t5$

3.2.4 LVDS Data and Control Signal Interface

The modules LVDS signals interface shall meet requirements of TIA/EIA-644. Figure 2 shows the data-mapping diagram of the/each LVDS channel.

3.2.4.1 LVDS Termination Impedance

The LVDS differential signals line-to-line termination impedance Z_T, shall be 100 $\pm$ 1ohms.

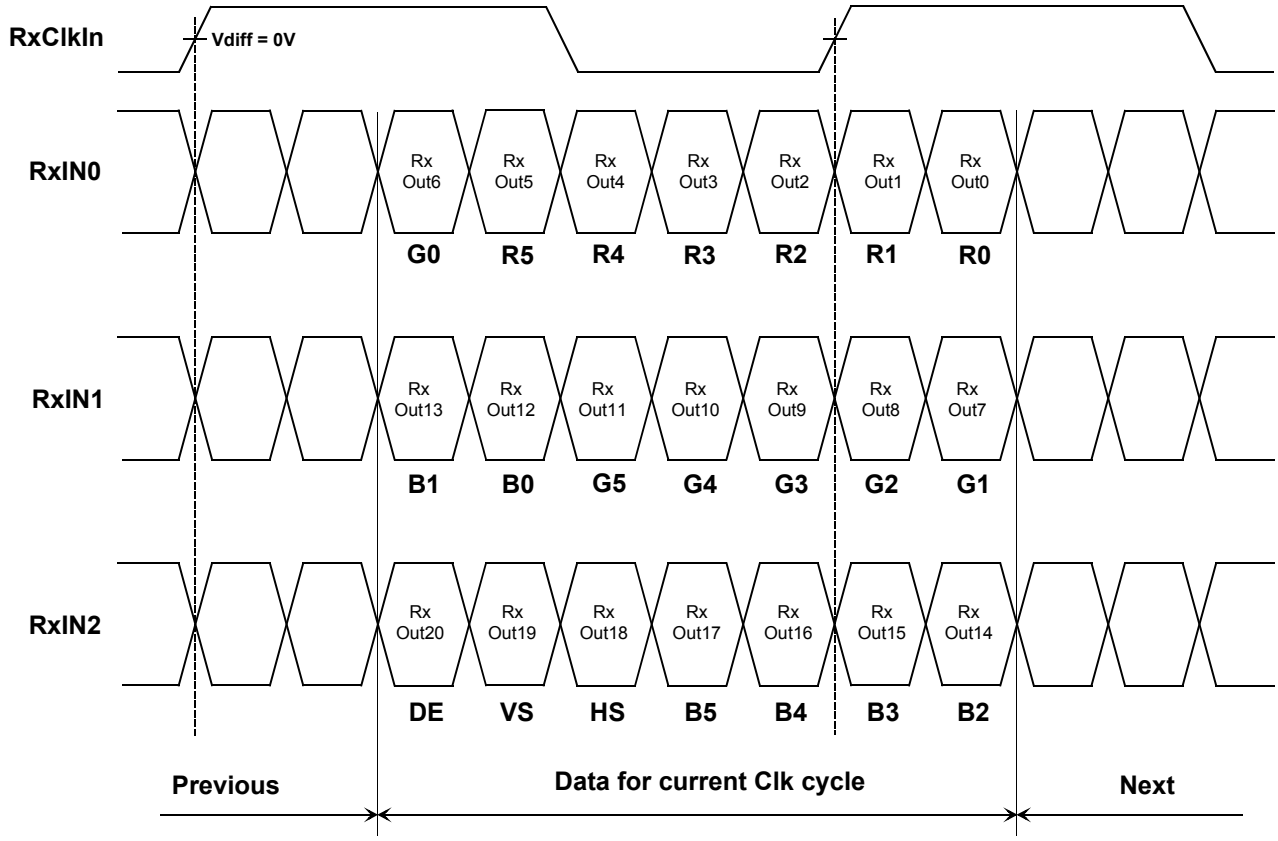
3.2.5 Backlight Electrical Interface

The panel-side backlight interface cable shall be terminated into a JST BHSR-02VS-1 as the recommended connector, or a JST BHTR-02VS as an alternative choice. The lamp wires exiting the panel shall be sufficiently protected so that normal movement of these wires during enclosure assembly will not cause the insulation to be cut. The connector interface pin assignments are listed in Table 4.

TABLE 4
BACKLIGHT ELECTRICAL INTERFACE

PIN NO.	SIGNAL	LEVEL	FUNCTION
1	V_{CFL}	AC	Power Supply for CFL
2	Gnd Rtn	~ GND	Power return for CFL

FIGURE 2
LVDS CHANNEL INTERFACE DATA MAPING DIAGRAM



4. MECHANICAL INTERFACE REQUIREMENTS

Figure 3 shows the pixel formatting for the active display surface. Figures 4, 5, and 6 show the critical exterior dimensions for the 13.3", 14.1" and 15.0" panels.

4.1 Style B Product Migration

It is strongly recommended that any new end-user applications (notebooks PCs, instrumentations, etc.) starting development in calendar year 2003, be designed around Style B based panel. This will aid both panel suppliers and end-users in managing EOL logistic and material issues.

4.2 Enabling Thinner Style B Modules

To support the development of both newer display technologies and ultra-thin displays, for modules that are too thin to reliably utilize mounting screws, these modules may be developed per the dimensions of Figures 4, 5, and 6 without incorporating the mounting holes. For these applications, the upper left mounting hole shall be replaced with a 0.5±0.1mm diameter reference locator hole, 2.0±0.3mm from the face of the module. Module dimensioning requirements shall be referenced off this locator hole.

FIGURE 3
ACTIVE AREA PIXEL LAYOUT

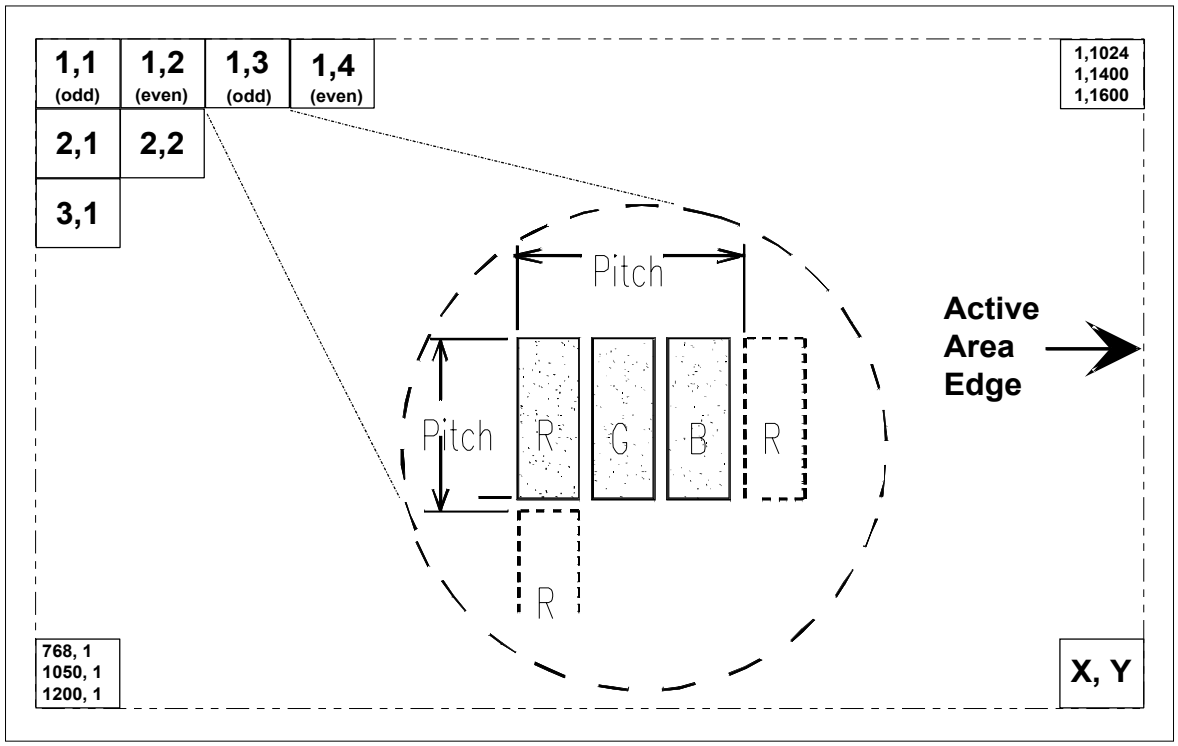


FIGURE 4
13.3" STANDARD PANEL CRITICAL DIMENSIONS

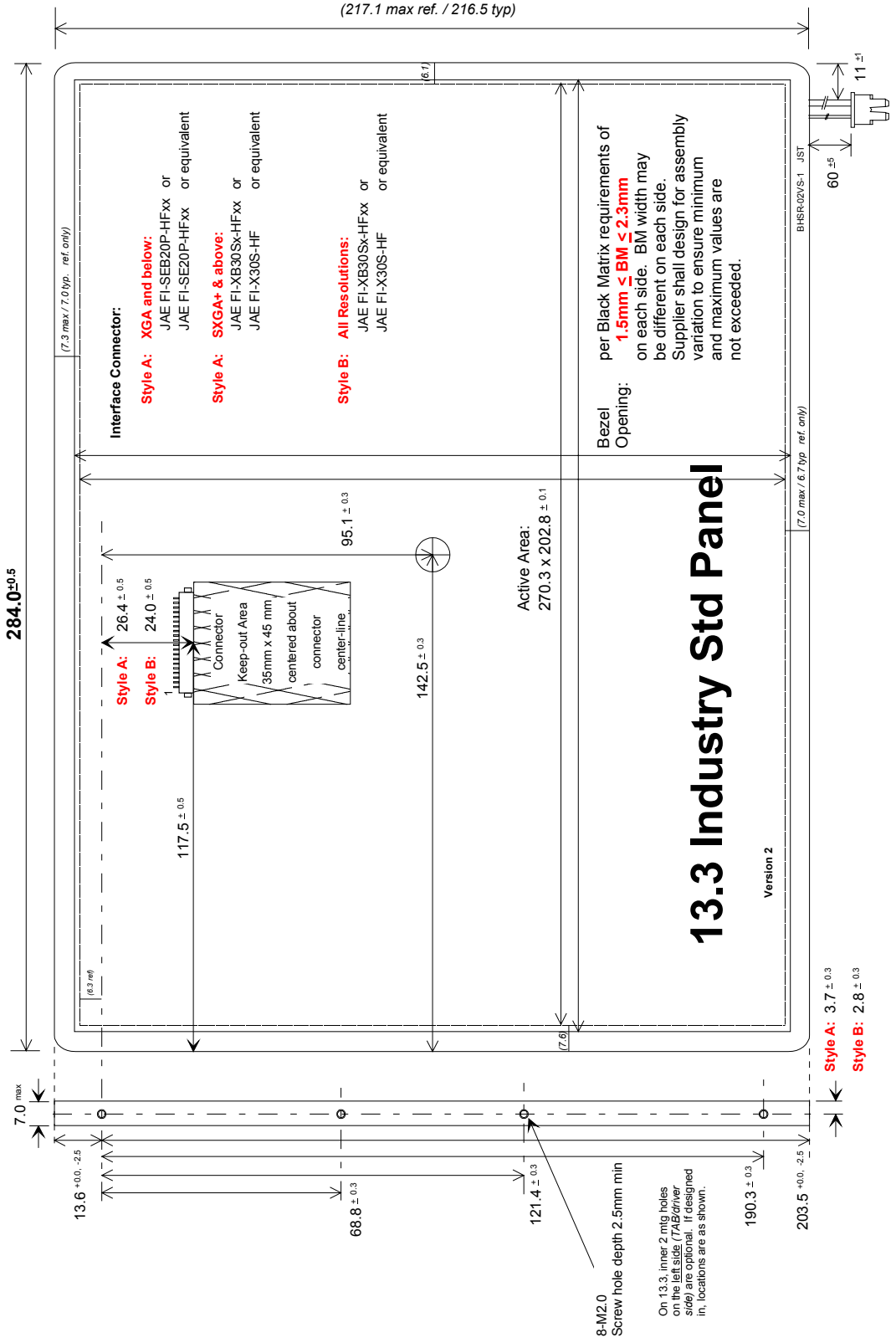


FIGURE 5
14.1" STANDARD PANELCRITICAL DIMENSIONS

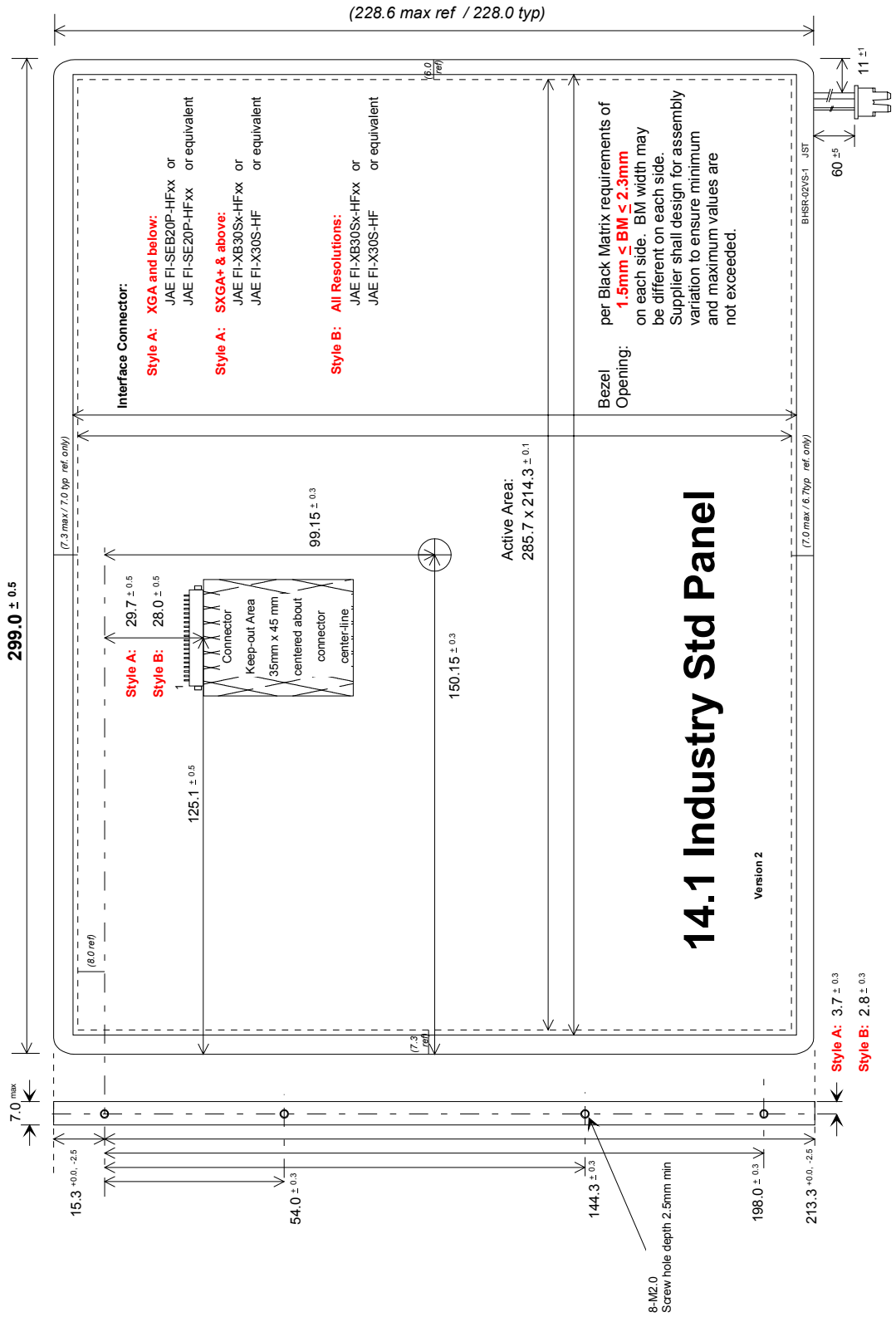
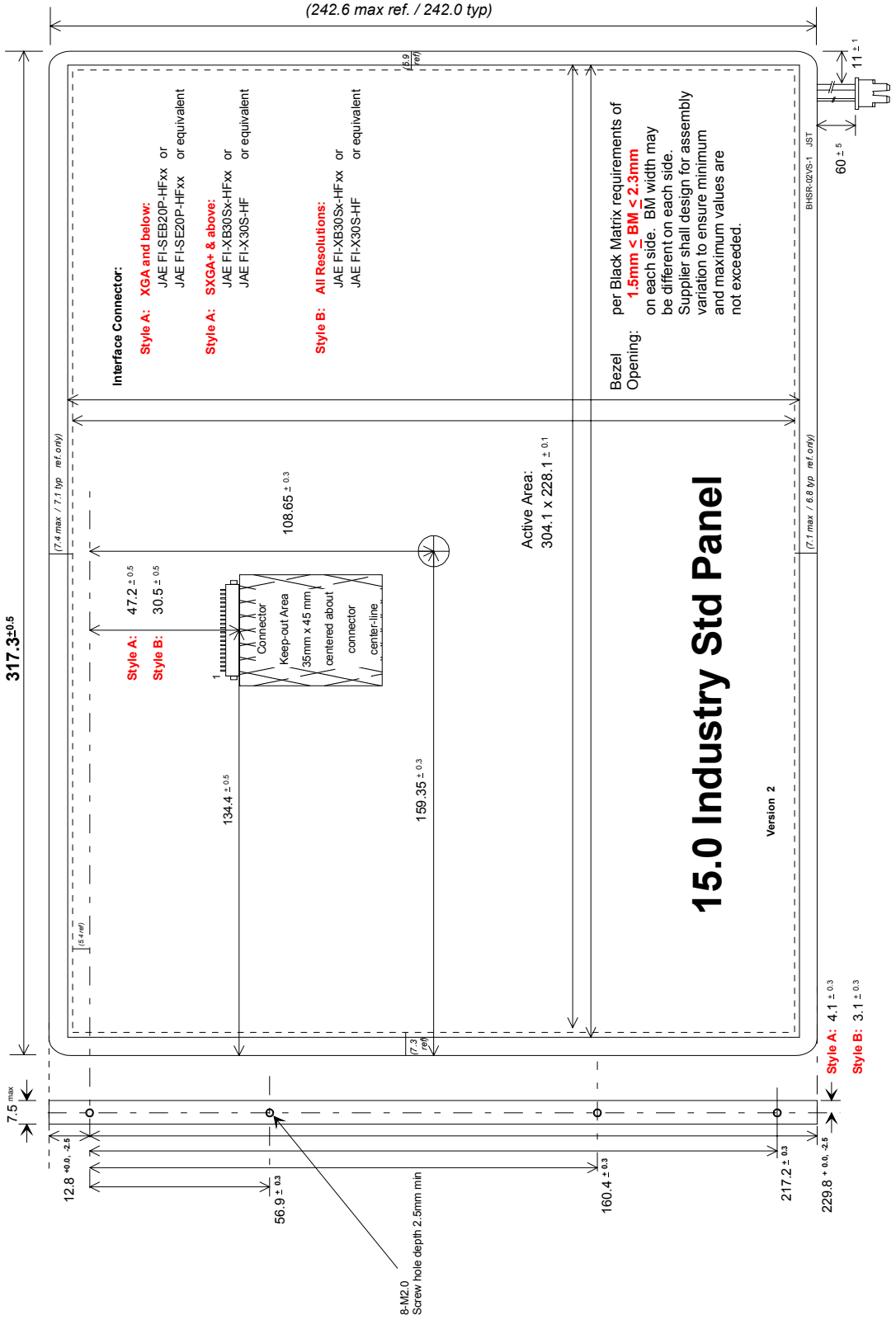


FIGURE 6
15.0" STANDARD PANEL CRITICAL DIMENSIONS



APPENDIX A - ISP Enhanced Extended Display Identification Data (E-EDID) Requirements

Byte# (dec)	Byte# (hex)	Field Name and Comments	Value (hex)	Value (binary)
		Header		
0	00		00	0000 0000
1	01		FF	1111 1111
2	02		FF	1111 1111
3	03		FF	1111 1111
4	04		FF	1111 1111
5	05		FF	1111 1111
6	06		FF	1111 1111
7	07		00	0000 0000
		Vender / Product ID / EDID Version		
8	08	EISA manufacturer code = *(1st byte)*		
9	09	*(2nd byte)*		
10	0A	Product code LSB =		
11	0B	Product code MSB =		
12	0C	ID (32-bit) serial number *(preferred, but optional, zero if not used)*		
13	0D			
14	0E			
15	0F			
16	10	Week of manufacture *(preferred, but optional, zero if not used)*		
17	11	Year of manufacture *(preferred, but optional, zero if not used)*		
18	12	EDID Structure version # = 1	01	0000 0001
19	13	EDID Revision # = 2	02	0000 0010
		Display Parameter		
20	14	Video input definition *(Digital I/P, non TMDS CRGB typ 80h)*	80	1000 0000
21	15	Max H image size (**xx**) *(rounded to cm)*		
22	16	Max V image size (**xx**) *(rounded to cm)*		
23	17	Display gamma = **x.x** *(=(gamma*100)-100)*		
24	18	Features *(no DPMS, Active off, RGB, timing BLK1)*	08	0000 1000

Panel Color Coordinates

25	19	Red/Green low Bits		
26	1A	Blue/White Low Bits		
27	1B	Red X Rx = 0.**xxx**		
28	1C	Red Y Ry = 0.**xxx**		
29	1D	Green X Gx = 0.**xxx**		
30	1E	Green Y Gy = 0.**xxx**		
31	1F	Blue X Bx = 0.**xxx**		
32	20	Blue Y By = 0.**xxx**		
33	21	White X Wx = 0.**xxx**		
34	22	White Y Wy = 0.**xxx**		

Established Timings

35	23	Established Timing I *(00h if not used)*		
36	24	Established Timing II *(00h if not used)*		
37	25	Manufacturer's Timings *(00h if not used)*		

Standard Timing ID

38	26	Standard Timing Identification 1 *(01h if not used)*		
39	27	Standard Timing Identification 1 *(01h if not used)*		
40	28	Standard Timing Identification 2 *(01h if not used)*		
41	29	Standard Timing Identification 2 *(01h if not used)*		
42	2A	Standard Timing Identification 3 *(01h if not used)*		
43	2B	Standard Timing Identification 3 *(01h if not used)*		
44	2C	Standard Timing Identification 4 *(01h if not used)*		
45	2D	Standard Timing Identification 4 *(01h if not used)*		
46	2E	Standard Timing Identification 5 *(01h if not used)*		
47	2F	Standard Timing Identification 5 *(01h if not used)*		
48	30	Standard Timing Identification 6 *(01h if not used)*		
49	31	Standard Timing Identification 6 *(01h if not used)*		
50	32	Standard Timing Identification 7 *(01h if not used)*		
51	33	Standard Timing Identification 7 *(01h if not used)*		
52	34	Standard Timing Identification 8 *(01h if not used)*		
53	35	Standard Timing Identification 8 *(01h if not used)*		

Timing Descriptor #1

54	36	Pixel Clock/10,000 *(LSB)*		
55	37	Pixel Clock /10,000 *(MSB)*		
56	38	Horizontal Active = **xxxx** pixels *(lower 8 bits)*		
57	39	Horizontal Blanking (**Thbp**) = **xxxx** pixels *(lower 8 bits)*		
58	3A	Horizontal Active : Horizontal Blanking(**Thbp**) *(upper 4:4 bits)*		
59	3B	Vertical Avtive = **xxxx** lines		
60	3C	Vertical Blanking (**Tvbp**) = **xxxx** (DE Blanking min for DE-only panels) lines		
61	3D	Vertical Active : Vertical Blanking(**Tvbp**) *(upper 4:4 bits)*		
62	3E	Horizontal Sync. Offset (**Thfp**) = **xxxx** pixels		
63	3F	Horizontal Sync Pulse Width = **xxxx** pixels		
64	40	Vertical Sync Offset (**Tvfp**) = **xx** lines, Sync Width = **xx** lines		
65	41	Horizontal Vertical Sync Offset/Width upper 2bits		
66	42	Horizontal Image Size = **xxx** mm *(lower 8 bits)*		
67	43	Vertical Image Size = **xxx** mm *(lower 8 bits)*		
68	44	Horizontal & Vertical Image Size *(upper 4:4 bits)*		
69	45	Horizontal Border *(zero for internal LCD)*	00	0000 0000
70	46	Vertical Border *(zero for internal LCD)*	00	0000 0000
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol negatives, DE only note *LSB is set to "1" if panel is DE-only timing (H/V can be ignored)*	18 *(19)*	0001 1000 *0001 1001*

Timing Descriptor #2 MANUFACTURER SPECIFIED RANGE TIMING Descriptor

72	48	Flag	00	0000 0000
73	49	Flag	00	0000 0000
74	4A	Flag	00	0000 0000
75	4B	Data Type Tag: **Descriptor Defined by Manufacturer**	0F	0000 1111
76	4C	Flag	00	0000 0000
77	4D	HSPW min (pixel clks)		
78	4E	HSPW max (pixel clks)		
79	4F	Thbp min (pixel clks) *(for DE-only timing also, with Thfp=0)*		
80	50	Thbp max (pixel clks) *(for DE-only timing also, with Thfp=0)*		
81	51	VSPW min (line pulses)		
82	52	VSPW max (line pulses)		
83	53	Tvbp min (line pulses)		
84	54	Tvbp max (line pulses)		
85	55	Thp min (pixel clks)		
86	56	Thp max (pixel clks)		
87	57	Tvp min (line pulses)		
88	58	Tvp max (line pulses)		
89	59	Module revision		

NOTE: SEE FIGURE A1 TIMING WAVEFORM PARAMETERS FOR DEFINITIONS

Timing Descriptor #3: ASCII String: Supplier Name

90	5A	Flag	00	0000 0000
91	5B	Flag	00	0000 0000
92	5C	Flag	00	0000 0000
93	5D	Data Type Tag: *(Monitor)* **ASCII String**	FE	1111 1110
94	5E	Flag	00	0000 0000
95	5F			
96	60			
97	61			
98	62			
99	63			
100	64			
101	65			
102	66			
103	67			
104	68			
105	69			
106	6A			
107	6B	*(if <13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)*		

Timing Descriptor #4: ASCII String: Supplier P/N

108	6C	Flag	00	0000 0000
109	6D	Flag	00	0000 0000
110	6E	Flag	00	0000 0000
111	6F	Data Type Tag: *(Monitor)* **ASCII String**	FE	1111 1110
112	70	Flag	00	0000 0000
113	71			
114	72			
115	73			
116	74			
117	75			
118	76			
119	77			
120	78			
121	79			
122	7A			
123	7B			
124	7C			
125	7D	*(if <13 char, then terminate with ASCII code 0Ah, and set remaining char = 20h)*		

126	7E	Extension Flag *(# of optional 128-byte EDID extension blocks to follow, typ=0)*		
127	7F	Checksum *(the 1-byte sum of all 128 bytes in this EDID block shall equal zero)*		

Figure A1. Timing Waveform Parameters